AMENDMENTS TO THE CLAIMS:

Please amend claims 11-13 and add new claims 22-25, as indicated below. This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1.-10. (Canceled)

11. (Currently Amended) A semiconductor device, comprising: ~~in which~~

a gate electrode of a MISFET formed on a semiconductor substrate [[is]] and electrically connected to a well region under a channel of [[said]] the MISFET,

wherein:

[[said]] the MISFET is formed on part of [[a]] at least one side surface of an island-shaped element region formed on [[said]] the semiconductor substrate,

the gate electrode of the MISFET is formed on at least part of the at least one side surface and an upper surface of the island-shaped element region, the upper surface being a surface of the well region; and

an electrical connection between [[said]] the gate electrode of [[said]] the MISFET and the well region in [[said]] the semiconductor substrate ~~is done~~ formed on [[an]] the upper surface of the island-shaped element ~~are electrically connected~~ region.

12. (Currently Amended) A semiconductor device according to claim 11, further comprising two gate electrodes connected electrically and formed on opposite side surfaces of the island-shaped element region.

13. (Currently Amended) A semiconductor device according to claim 12, further comprising [[a]] source and drain regions formed ~~to sandwich said each gate electrodes formed on said opposite sides~~ on opposite side surfaces of the island-shaped element region, the source and drain regions being formed on at least one side of each of the two gate electrodes.

14. (Withdrawn) A semiconductor device comprising:

a semiconductor substrate including an island-shaped element comprised of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area parallel to a surface of said substrate than that of said lower structure;

a pair of gate insulating films formed on opposing sides of said lower structure of the element region, respectively;

a sidewall insulating film formed on a side surface of said upper structure of the element region;

a gate electrode formed on said pair of gate insulating films, an upper surface of said sidewall insulating film, and an upper surface of said upper structure of the element region; and

source and drain regions formed on opposite side surfaces of said lower structure of the element region so as to sandwich said pair of gate insulating films, wherein bottom surfaces of said source and drain diffusion layers formed on side surfaces of the element region are in contact with each other.

15.-21. (Canceled)

22. (New) A semiconductor device according to claim 13, wherein bottom surfaces of the source and drain regions are in contact with each other.

23. (New) A semiconductor device, comprising:

an island-shaped element region including a well region formed on a substrate, the island-shaped element region having side surface regions opposite to each other and an upper surface formed between the side surface regions, the upper surface being a surface of the well region; and

gate electrodes of at least one MISFET formed over the side surfaces and the upper surface of the island-shaped element region,

wherein the gate electrodes are electrically connected to the well region.

24. (New) The semiconductor device according to claim 23, further comprising source and drain regions formed on the side surfaces of the island-shaped element region and at least one side of each of the gate electrodes.

25. (New) The semiconductor device according to claim 24, wherein bottom surfaces of the source and drain regions are in contact with each other.